RESEARCH INVENTY: International Journal of Engineering and Science
ISSN: 2278-4721, Vol. 1, Issue 7 (November 2012), PP 19-24
www.researchinventy.com

Effect of ESD on Data in a Digital Switching Circuit

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Abstract *- The behavior of the digital data from digital switching circuit when subjected to Human Body Model (HBM) of the Electrostatic Discharge (ESD) is analyzed. Indirect discharge has been conducted in both the horizontal coupling plane (HCP) and vertical coupling plane (VCP). The results show that the data gets affected based on the position of occurrence of trigger or transient pulse and the coupling plane. The distance at which the pulse is discharged also plays an important role on the amplitude of the transient. The discharge in the VCP affects the digital data more than the discharge in the HCP. When the varying coupling capacitors are used it is seen that smaller the value of the coupling capacitor, more susceptible the circuit becomes to ESD.*

Keywords *- Electrostatic Discharge; Human Body model; Electromagnetic radiated fields; ESD simulator; Electromagnetic Interference; Integrated Circuit*

I INTRODUCTION

Malfunctioning of Integrated Circuits (IC) and electronic systems have been mathematically predicted for the circuits exposed to the radiated field [1, 2] generated by indirect discharge from an ESD simulator [3]. Even with suitable ESD protection circuits in the integrated circuits, the IC's are still damaged by the ESD discharge [4, 5]. The problem of protection becomes more serious in the circuits which have IC's not protected with the right value of decoupling capacitors [6, 7, 8] at their V_{cc} terminal.

The ESD indirect discharge test was carried out to verify the ESD immunities of the integrated circuits used in the circuit generating an output of specified data stream. Indirect discharge on the HCP and VCP is performed. An ESD transient has been introduced momentarily in the clock and data stream and its effect on the ones and zeroes of the specified data stream has been observed. The ESD transient introduced affected the data stream and clock depending on the occurrence of the transient in the bit stream. Also an effective ESD protection solution in the form of right value for the decoupling capacitors has been studied for improving the ESD robustness of the integrated circuits used in the electronic systems.

II CIRCUIT DIAGRAM AND ITS OPERATION

The circuit shown in Fig. 1 consists of a 555 timer working as an astable multivibrator (NE555), Hex inverter buffer (IC74LS14), dual 4 stage binary counter (IC74LS393), monostable multivibrator (IC 74LS121), 8 bit Parallel In Serial Out (PISO) shift register (IC 74LS165) and an 8-way DIP switch.

The astable multivibrator is used to produce a clock with a frequency in the range 62.5 KHz to 118 KHz. This clock is given as the input to the binary counter which is configured to work as a divide by 8 counter. The output of the binary counter is fed to the monostable multivibrator which triggers the parallel to serial conversion in the shift register by sending a low pulse to the active low enable pin of the PISO shift register after every 8 clock pulses. The clock input to the shift register is fed from the astable multivibrator. Data on the parallel data lines from the DIP switch is converted to serial data and is available on the data output pin. The 8 data bits is followed by a series of eight 1's or eight 0's depending on whether the last switch of the DIP is high or low.

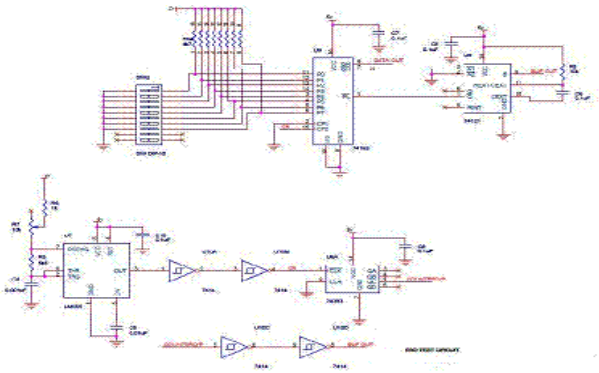

Fig. 1 Digital switching circuit

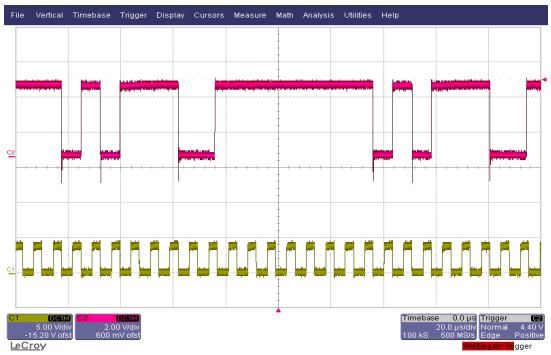

Fig. 2 Initial output of clock and data

III EFFECT OF INDIRECT ESD

The initial output of the clock and the data is shown in Fig. 2. The waveform at the top represents the serial data and the waveform at the bottom represents the clock.

Horizontal Coupling Plane (HCP)

Indirect discharges at different voltages and distances have been conducted. The result for a discharge of 8kV at a distance of 0.6m from the circuit is given below. During the discharge if the data and the clock are triggered at a low there is an occurrence of a ringing transient at the data and the clock as shown in Fig. 3. It can be seen that the transient of about 15V affects the data for 2µs.

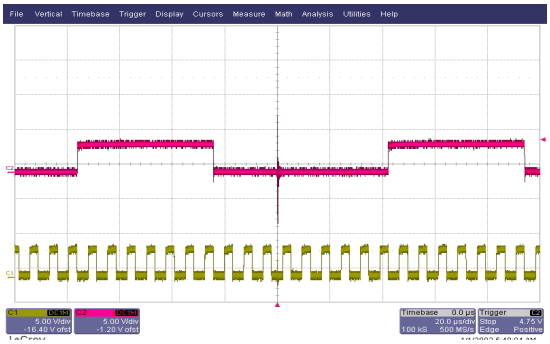

Fig. 3 Output when data and clock are triggered at low

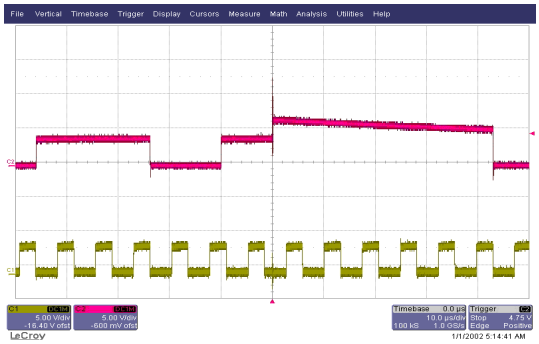

Fig. 4 Output when data is triggered at high and clock is triggered at low.

There is an increase in the amplitude of the data till the next low bit and a small transient is present at the clock in the point of occurrence of the discharge when the data is triggered at a high and clock is triggered at a low shown in Fig. 4. A ringing transient of 15V occurs for 2µs in the data and an increase in amplitude of the clock in the same time period is observed as shown in Fig. 5 when the data is triggered at a low and the clock is triggered at a high.

Fig, 5 Output when data is triggered at low and clock is triggered at high.

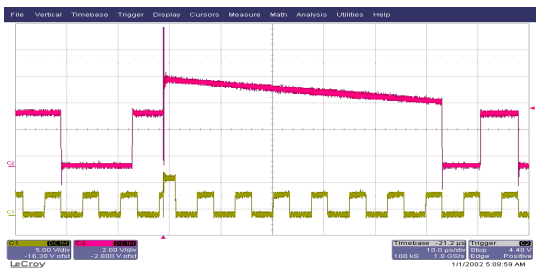

Fig. 6 Output when data and clock are triggered at a high

The amplitude of the data either increases till the next low bit of the data or the data inverts till the next low clock pulse when the data and clock are triggered at a high. Further it can be noticed that there is an increase in the amplitude of the clock pulse from the point of trigger till the next clock low as shown in Fig. 6 and Fig. 7.

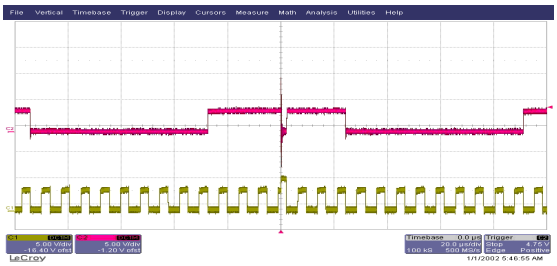

Fig. 7 Output when data and clock triggered at a high

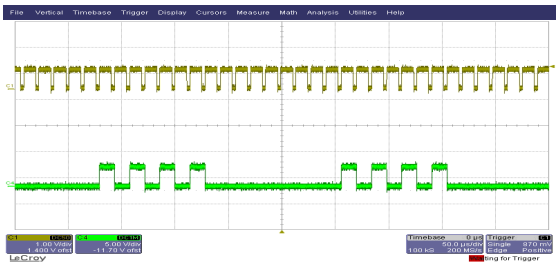

Fig. 8 The initial output of clock and data

Vertical Coupling Plane (VCP)

A discharge of 4kV was given at the 4 corners of the vertical coupling for all the results discussed below. Also different voltages were discharged on the corners of VCP. The initial output for the clock and the data for the vertical coupling plane is shown in Fig. 8. When discharged at the top right corner of the VCP a transient of 40V at the clock and 55V at the data at the point of discharge and also a loss of data from the point of the discharge was observed. This is shown in Fig. 9.

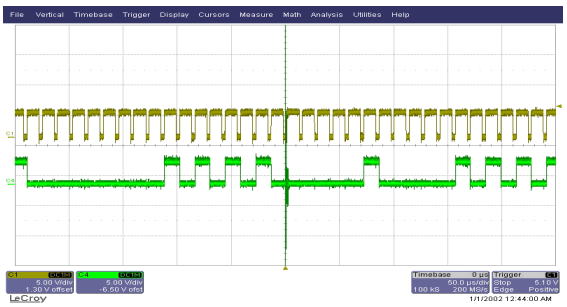

Fig. 9 Output when discharged at top right corner of VCP.

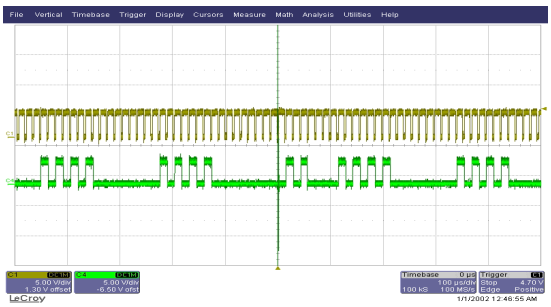

Fig. 10 Output when discharged at bottom right corner of VCP.

A transient of 50V at the clock and 55V at the data was observed with a loss of data in the following cycle when discharged at the bottom right corner of the VCP. This is shown in Fig. 10. A transient of 50V at the clock and 55V at the data was observed with a loss of data in the following cycle when discharged at the top left corner of the VCP. This is shown in Fig. 11.When discharged at the bottom left corner of the VCP a transient of 40V at the clock and 55V at the data at the point of discharge and also a data loss is observed. This is shown in Fig. 12.

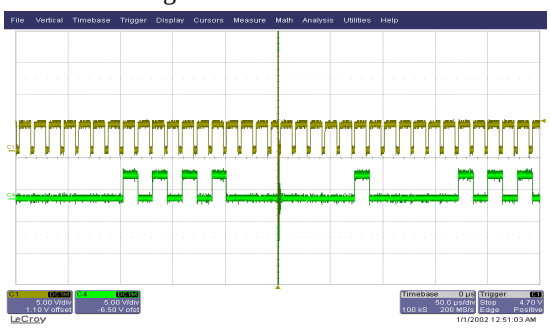

Fig. 11 Output when discharged at top left corner of VCP.

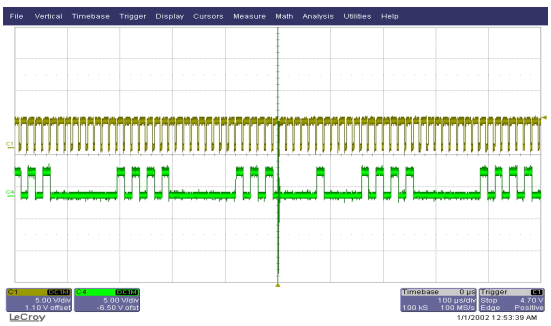

Fig.12 Output when discharged at bottom left corner of VCP

IV. Effect of ESD on the Digital Switching Circuit without Coupling Capacitors

The initial output of the digital switching circuit without the coupling capacitors is shown in the Fig. 13.

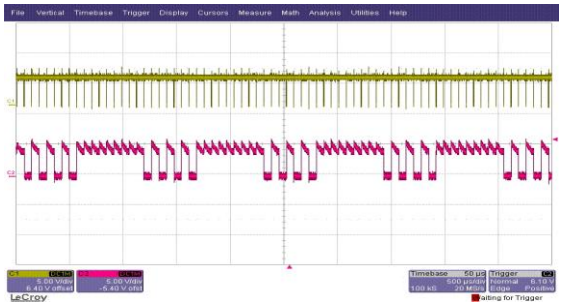

Fig. 13 Initial output of clock and data

Fig. 14 Output after a discharge of a 15kV at a distance of 0.9m

For an air discharge of 15kV at a distance of 0.9m there was more than 40V transient in the data and around 5V transient in the clock along with data loss as shown in the Fig. 14. When an air discharge of 15kV was done at a distance of 0.75m there was more than 38V transient in the data and around 7V transient in the clock along with data loss of more than 8 bits as shown in the Fig. 15. When an air discharge of 15kV was done at a distance of 0.5m there was more than 12V transient in the data and around 2V transient in the clock along with data loss as shown in the Fig. 16.

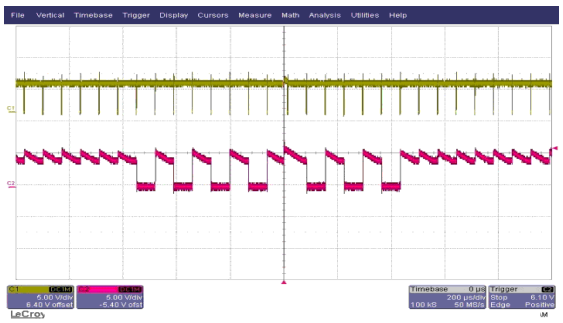

Fig. 15 Output after a discharge of a 15kV at a distance of 0.75m

Fig. 16 Output after a discharge of a15kV at a distance of 0.5m

When an air discharge of 15kV was done at a distance of 0.3m there was a 45V transient in the data and around 6.5V transient in the clock as shown in the Fig. 17. For an air discharge of 15kV at a distance of 0.3m there was also an increase in the amplitude of the data as shown in the Fig. 18.

Fig. 17 Output after a discharge of a 15kV at a distance of 0.3m

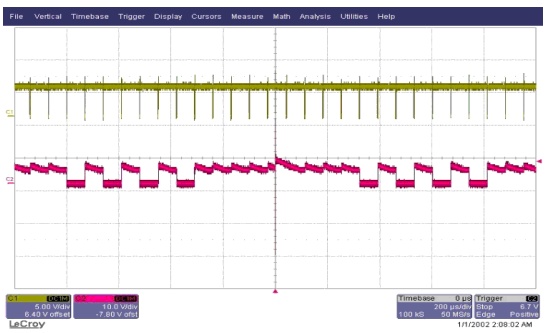

Fig. 18 Output after a discharge of a 15kV at a distance of 0.3m

For an air discharge of 15kV at the 555 timer output there was more than 80V transient in the data and more than 80V transient in the clock and the output remains constant momentarily and later resumes with reduced amplitude as shown in the Fig. 19.

Fig. 19 Output after a discharge of a 15kV at the 555 timer output

Fig. 20 Output for 0.001µf coupling capacitor

V. EFFECT OF ESD ON DIGITAL SWITCHING CIRCUIT WITH VARYING COUPLING CAPACITORS

For the same circuit we use different values of coupling capacitors and verify the susceptibility of the circuit to ESD for each capacitor value. The values of coupling capacitors chosen are 0.47µf, 0.1µf, 0.047µf, 0.01µF and 0.001µf in the decreasing order of their value. An indirect discharge of 15kV on the horizontal coupling plane at a distance of 0.5m from the circuit was given for all the results given below.

When ESD indirect discharge is performed at the circuit with 0.001µf there is a large transient of about 20V at the clock but as the data is at low there is not much effect on the data output. This is shown in Fig. 20. For a circuit with a coupling capacitor value of 0.01µf the discharge causes a large transient in the clock and also there is loss of data with more than 4 bits being lost as shown in the Fig. 21.

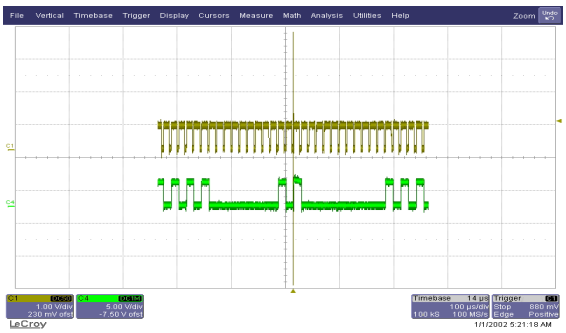

Fig. 21 Output for 0.01µf coupling capacitor

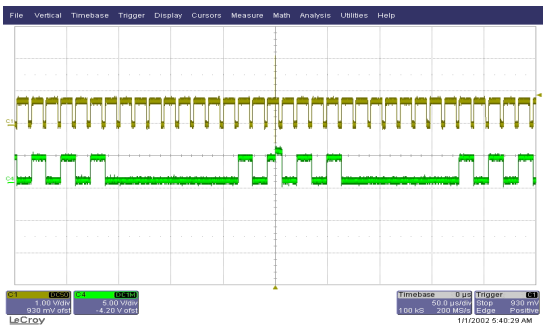

Fig. 22 Output for 0.047µf coupling capacitor

When discharged on the circuit with the value of the coupling capacitor equal to 0.047µf the data had an 2V increase in the amplitude and also there was a 15V taransient in the clock output at the point of trigger as shown in the Fig. 22. For 0.1µf capacitor the discharge produced a 1V increase in the data and a transient of 5V in the clock was introduced at the point of trigger as shown in the Fig. 23. For 0.47µf the amplitude of the data is increased by 0.5V and that of the clock by 0.5V as shown in the Fig. 24. It can also be seen that there are no transients at the point of discharge.

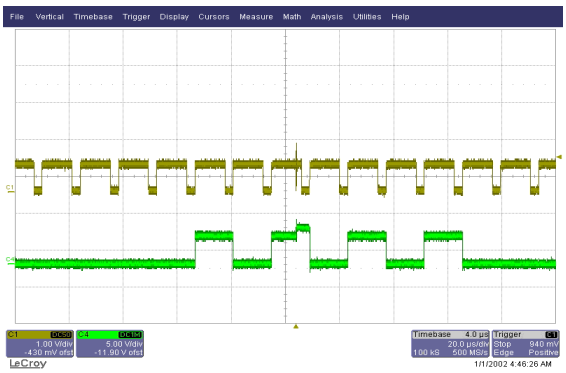

Fig. 23 Output for 0.1µf coupling capacitor

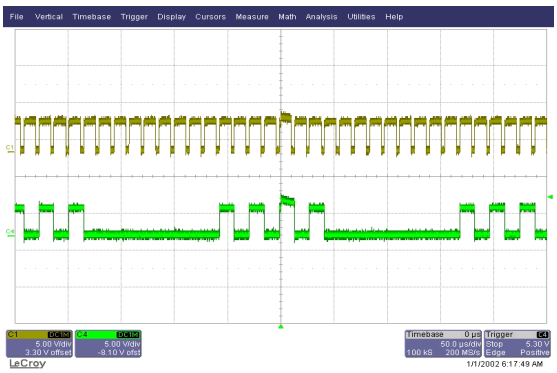

Fig. 24 Output for 0.47µf coupling capacitor

VI COMPARISON AND CONCLUSION

We can see that the response of the data in a digital switching circuit to ESD depends on position of trigger and also the plane of coupling. From the results in the horizontal plane we can conclude the position of the trigger plays an important role in the effect of ESD. This effect is tabulated in Table 1. The distance at which the pulse is discharged plays an important role on the amplitude of the transient.

Clock	Data	Effect
Low	Low	Ringing transient
Low	High	Increase in the amplitude of data and transient in the clock
High	Low	Transient in the data and a amplitude shift at the clock
High	High	Amplitude shift or inversion in the data and increase in the amplitude of the clock

Table 1. Comparison of the result with respect to point of occurrence of the discharge.

In the Vertical Coupling Plane there is a loss of data and also a huge transient of about 55V in the data and a transient of about 40 to 50V in the clock is observed. We can conclude that the discharge in the VCP affects the digital data more than the discharge in the HCP.When the varying coupling capacitors are used it is seen that smaller the value of the coupling capacitor the circuit becomes more susceptible to ESD. It can be seen from the results that the capacitor with a higher value of capacitance gives better immunity to ESD because of its ability to pass only lower frequencies thereby rejecting the high frequency ESD transients and shifting the cut off to as close to DC as possible.

REFERENCES

[1] Rajashree Narendra, M.L.Sudheer, V. Jithesh, D.C. Pande, "Mathematical Analysis of ESD Generated EM Radiated Fields on Electronic Subsystem", *Asia Pacific Symposium on EMC, 2010, pp. 449-452.*

[2] S.V.K. Shastry and V.K. Hariharan, "Computer Aided Analysis Of ESD Effects In Dual Gate MOSFET VHF Amplifier", *IEEE International Symposium on EMC, Aug 1990, pp. 424-430.*

[3] Robert Ashton, "System level ESD Testing-The Test setup"**,** *Challenges in testing, Conformity, December 2007, pp 34-40.*

[4] Ming-Douker, Jeng-Jie Peng and Hsin-Chin Jiang, "Failure Analysis of ESD damage in a high-voltage driver IC and the effective ESD protection solution", *Proceedings of 9th IPFA 2002, Singapore, pp 84-89.*

[5] C. Duvvury, R.N.Rountree and O. Adams, "Internal chip ESD phenomena beyond the protection circuit", *IEEE Transactions on Electron Devices, Vol. 35, No. 12, 1988, pp 2133-2139.*

[6] Zhen Mu and Heiko Dudek, Kun Zhang*, *"How to Choose & Place Decoupling Capacitors to Reduce the Cost of the Electronic Products",* Cadence Design Systems, Inc., * Huawei Technologies Co., Ltd, 2003.

[7] Hubing, Van Doren, Sha, Drewniak, and Wilhelm, "An Experimental Investigation of 4-Layer Printed Circuit Board Decoupling", *Proceedings of the 1995 IEEE International Symposium on Electromagnetic Compatibility, August, 1995, pp. 308-312.*

[8] Tamara Schmitz and Mike Wong, *"Choosing and Using Bypass Capacitors",* INTERSIL Application Note, AN1325.0, August 3, 2007, pp. 1-10.